IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		)	
	Knall *et al.*	)	
		)	Examiner: Jennifer M. Dolan
Serial No.:	10/689,187	)	
		)	Group Art Unit: 2813
Filed:	October 20, 2003	)	
		)	Docket No: SD-MA-002-1-I-a
For:	Three-Dimensional Memory Array and Method of Fabrication	)	

AMENDED APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 7, 2008

This Amended Appeal Brief is being filed in response to the Final Office Action mailed April 17, 2006, as well as the Notice of Non-Compliance With The Requirements of 37 CFR 41.37(c) mailed March 6, 2008, and the Order Returning Undocketed Appeal to Examiner, mailed November 20, 2007.

A Petition For Extension Of Time Under 37 C.F.R. §1.136 and the appropriate fee were submitted previously with the original Appeal Brief on October 17, 2006. As this Amended Appeal Brief is being filed within one month of the mailing date of the above-mentioned Notice of Non-Compliance, Applicants do not believe that a Request for Extension of Time is required, but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696.

The fee set forth in 1.17(c) has been submitted previously. Applicants do not believe that any additional fees are due regarding this Amended Appeal Brief. However, if any additional fees are required, please charge Deposit Account No. 04-1696.

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I. Real Party in Interest

SanDisk 3D LLC is the real party in interest.

II. Related Appeals and Interferences

An Appeal Brief has been filed in US Patent Application 10/610,804, filed June 30, 2003, hereinafter the '804 application. The '804 application is a continuation-in-part of US Patent Application No. 10/153,999, hereinafter the '999 application. The present application is a continuation of the '999 application. The same Examiner is examining both the '804 application and the present application, and there are references in common.

III. Status of Claims

Claims 1 and 2 are pending in the application. Claims 1 and 2 stand rejected and are the subject of this appeal.

IV. Status of Amendments

No amendments were filed subsequent to the final rejection.

V. Summary of Claimed Subject Matter

The present application describes a memory array comprising memory cells, each memory cell comprising an antifuse.

Antifuses are known elements in semiconductor devices. An antifuse separates a conductor or semiconductor from another conductor or semiconductor, and is characterized by having two states. Initially electrically insulating, when an antifuse is subjected to a high current, it ruptures and becomes conductive, and remains so permanently.

An antifuse, in its intact state, can serve to prevent electrical contact between two metal or metallic conductors. When the antifuse is ruptured, an electrical contact is formed between the conductors. Such an antifuse is a *conductor-to-conductor* antifuse. A conductor-to-conductor

antifuse may be used in, for example, an LPGA to switch a circuit on, i.e., to make it active by forming a contact to it when the antifuse is ruptured.

Its two possible distinct states, isolating or conductive, also make an antifuse useful in a nonvolatile memory cell, as in the present invention. A cell containing, or isolated from a conductor by, an antifuse in an intact, insulating state may be considered to correspond to a zero or a one, while the same cell with a ruptured, conductive antifuse corresponds to the opposite value. One data state allows significant current flow under applied voltage, while the other does not, allowing each state to be reliably detected. This property remains whether power is applied to the device or not.

There are many types of nonvolatile memory cells, some of which incorporate, for example, transistors, tunnel junctions, etc. In some memory cells, an antifuse is paired with a diode.

A diode allows current to flow more easily in one direction than the other. Two types of diodes commonly used in diode-antifuse memories are p-n diodes and Schottky diodes. In a p-n diode, p-type semiconductor material is adjacent to n-type semiconductor material. Silicon is the most commonly used semiconductor material. A Schottky diode is formed when a semiconductor material is adjacent to a metal. In prior art devices, a diode paired with an antifuse has been fabricated in which the antifuse is formed of, for example, silicon dioxide, a known, high-quality dielectric.

In the present invention, an antifuse in a memory cell is formed of silicon nitride. The K-value of a dielectric is a measure of its quality as an insulator. Silicon nitride is a high-K dielectric, which means that a silicon nitride antifuse will generally allow more current to flow

under a given applied voltage than will an antifuse of comparable thickness formed of a lower-K dielectric material like silicon dioxide.

Leakage current in memory cells in a memory array is undesirable because it wastes power, and because, when current flow is used to distinguish a programmed cell from an unprogrammed cell, leakage current makes this distinction more difficult. When addressing a selected memory cell within a dense memory array, neighboring unselected cells will unavoidably be subjected to voltage, and must survive this voltage without accidental rupture. Because of these and other disadvantages, Appellants are not aware of the use of silicon nitride as an antifuse material in a diode-antifuse memory cell, or in fact in any memory cell, prior to the present invention.

Independent claim 1 recites a three dimensional multi-level memory array disposed above a substrate, the array comprising: a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate; a second plurality of spaced-apart rail-stacks disposed above the first height and in a second direction different from the first direction; and a plurality of memory cells, each memory cell comprising a silicon nitride antifuse, wherein the antifuses are disposed at the intersections of the first rail-stacks and the second rail-stacks. One possible embodiment is shown in Fig. 1 of the present application. The first railstacks include layers 21 through 24, while the second railstacks include layers 28 through 31. Alternatively, the first railstacks may be considered layers 14 through 15, while the second railstacks are considered to be layers 21 through 24. All of these layerstacks are formed over substrate 10. As described in paragraph [0024], in this embodiment, memory cells are formed where railstacks intersect. For example, one memory cell is present between the rail-stacks and layers shown within the bracket 17, while another is within the bracket 19. Each of these memory cells

includes an antifuse; for example, the memory cell defined within bracket 17 includes antifuse 26, while the memory cell defined within bracket 19 includes antifuse 20. As described in paragraph [0029], this antifuse may be formed of silicon nitride.

VI. Grounds of Rejections to Be Reviewed on Appeal

There are two grounds of rejection to be reviewed on appeal:

A. Independent claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Zhang, US Patent No. 5,835,396 (hereinafter Zhang '396), in view of Zhang et al., US Patent No. 6,111,302 (hereinafter Zhang '302). Appellants assert there is no motivation to make the suggested combination.

B. Independent claim 1 and its dependent claim 2 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Zhang '396 in view of Mohsen et al., US Patent No. 4,881,114. Appellants assert there is no motivation to make the suggested combination.

VII. Argument

An argument relating to each of the two grounds of rejection listed in Section VI above will be presented.

A. Rejection Over Zhang '396 in View of Zhang '302

Appellants respectfully submit that the rejection of claim 1 under 35 U.S.C. §103(a) over the proposed combination of Zhang '396 and Zhang '302 should be removed for the reasons set forth below.

In the Office action of April 17, 2006, The Examiner asserts (page 3) that it would have been obvious to one of ordinary skill in the art to use the silicon nitride antifuse of Zhang '302 in the memory cell of Zhang '396, saying that they have "generally similar materials and similar

structures." The Examiner further suggests the additional motivation that a silicon nitride antifuse, formed in the structure of Zhang '302, prevents switch-off. Appellants will show that one skilled in the art would not have been motivated to make the suggested combination.

As described in Zhang '302, as formed, an antifuse is insulating. Upon application of a programming voltage, the antifuse is ruptured, and a conductive rupture region is formed through it. In some structures, this conductive region may degrade over time, such that the antifuse is no longer conductive, and reverts to its original, non-conductive state. This phenomenon is called switch-off. The purpose of Zhang '302 is to prevent switch-off. (Col. 3, line 39 - col. 4, line 16).

Zhang '302 is clearly speaking of a *conductor-to-conductor* antifuse (see Abstract, col. 1, lines 15-18, and throughout), disposed between two metal or metallic conductors. When the antifuse is intact, there is no electrical connection between top conductor 22 and bottom conductor 14 of Fig. 1. When the antifuse is ruptured, a connection is made between these two conductive layers.

Zhang '302 addresses the problem of switch-off by forming conductors 14 and 22 of high thermal resistance materials. This causes the rupture region formed through antifuse 20 to be larger and more durable (col. 5, lines 26-46). Named preferred materials for these conductors have thermal conductivities below 0.4 W cm^{-1} K^{-1} (col. 5, line 38).

In Zhang '396, embodiments that include antifuses are shown in Figs. 9a through 10b (col. 9, lines 9-20). For clarification, Appellants note that Figs. 5a-6e show MPROM embodiments, which do not include an antifuse.

The embodiments shown in Figs. 9a through 9c all include an EPROM layer 502c between conductors 501 and 503. Conductors 501 and 503 are not formed of high thermal resistance layers, as taught in Zhang '302. Rather these conductors are formed of metals, and the

preferred metals of Zhang '396 are aluminum and copper (col. 5, lines 17-29), both of which are low-thermal resistance materials. Referring to Zhang '302, in Table 1 at col. 5, it will be seen that the thermal conductivities of aluminum and copper are 2.37 cm^{-1} K^{-1} and 4.01 W cm^{-1} K^{-1}, respectively, far above the preferred range of Zhang '302, which is below 0.4 W cm^{-1} K^{-1}. (Note that thermal resistance and thermal conductivity are inversely proportional; a low thermal resistance layer has high thermal conductivity).

Further, in the embodiments of Figs. 9a through 9c, at least one other layer exists in addition to the antifuse 502ca between conductors 501 and 503. In Fig. 9a, quasi-conduction layer 502cb (an amorphous silicon or protective ceramic layer) is included (col. 9, lines 21-40). In Fig. 9b, n-doped silicon layer 502cba and p-doped silicon layer 502cbb form p-n diode 502cb, which is also between conductors 501 and 503, along with antifuse layer 502ca (col. 9, lines 41-51). In Fig. 9c (col. 9, lines 52-64), between antifuse layer and bottom conductor 503 are quasi-conduction layer 502cb and a buffer layer 502cc, which is preferably of tungsten (col. 9, line 57), another low-thermal resistance material *not* preferred by Zhang '302 (see Table 1 of Zhang '302, col. 5). To summarize, each of these embodiments includes low thermal resistance top and bottom conductors 502 and 503 (different from the high thermal resistance top and bottom conductors 14 and 22 of Zhang '302), and at least some other layer, either a quasi-conduction layer, a p-n diode, or a quasi-conduction layer *and* a buffer layer, all unlike the simple conductor-to-conductor antifuse of Zhang '302.

The embodiments of 10a and 10b are also structurally and electrically dissimilar to those of Zhang '302. The structures of both Figs. 10a and 10b include the elements of Fig. 9c: Between conductors 501 and 503 are quasi-conduction layer 502cb, buffer layer 502cc (formed of tungsten, a low-thermal resistance layer), along with antifuse 502ca (col. 10, lines 7-26).

None of these embodiments shows a simple silicon nitride layer between high thermal resistance metal layers 14 and 22 as in Fig. 1 of Zhang '302. (Note that layers 16 and 21 are thin metallic barrier layers, see col. 5, lines 63-64, and col. 7, lines 32-42).

The Examiner suggested that the structures and materials of Zhang '396 and Zhang '302 are similar and thus a substitution of the silicon nitride of Zhang '302 for the antifuse of Zhang '396 would be obvious; as Appellants have just shown, they are not. An additional motivation provided by the Examiner to make the combination is to prevent switch-off in Zhang '396. But the structure the Examiner suggests, putting the silicon nitride antifuses in Zhang '396, does not avoid switch-off, since the high thermal resistance layers suggested by Zhang '302 do not appear in Zhang '396. Further, Appellants respectfully note that Zhang '302 describes the switch-off phenomenon as a problem in *conductor-to-conductor* antifuses; there is no suggestion that switch-off is also a problem in memory cells, the device described by Zhang '396. There is no mention of the problem of switch-off in Zhang '396, nor any stated desire for a solution. Appellants respectfully assert that one skilled in the art would have had no motivation to make the combination suggested by the Examiner.

B. Rejection Over Zhang '396 in View of Mohsen et al.

Appellants respectfully submit that the rejections of claims 1 and 2 under 35 U.S.C. §103(a) over the proposed combination of Zhang '396 and Mohsen et al. should be removed for the reasons set forth below.

The Examiner finds all of the elements of claim 1 in Zhang '396 except the claimed silicon nitride antifuse. The Examiner suggests that one skilled in the art would find it obvious to replace the antifuse of Zhang '396 with a silicon nitride antifuse as disclosed in Mohsen et al., again finding the environments in which the antifuses operate to be similar.

The Examiner maintains (at the bottom of page 4) that Mohsen et al. show "that silicon nitride is an appropriate antifuse for use between metal electrodes or metal and semiconductor electrodes ..." For this teaching the Examiner relies on the following passage at col. 4, lines 4-10 of Mohsen et al.:

> Both of the semiconductor materials used to form electrodes 12 and 16 may be made up of a high electromigration immunity material. They may be formed from heavily doped polysilicon, or heavily doped single crystal silicon or a metal or a sandwich of metal and heavily doped polysilicon in the alternative embodiment.

The Examiner has apparently interpreted this passage to mean that either layer 12 or 16 (which are separated by antifuse layer 14) can be any of the named materials: doped polysilicon, doped single-crystal silicon, or metal. In light of all of the other teachings provided by this patent, however, Appellants respectfully suggest that this interpretation does not seem reasonable.

In every description of the invention and described embodiments, including in the abstract, the claims, the summary, Figs. 1-3 and 9a-10b, and at every other point in the detailed description, it is made clear that rupture of the antifuse layer forms a diode; that is, that the antifuse initially separates layers that will form a diode when they are brought in contact upon rupture of the antifuse. In most embodiments, then, the antifuse separates an n-doped semiconductor layer from a p-doped semiconductor layer, forming a p-n semiconductor diode only when the antifuse is ruptured. In Fig. 1 of Mohsen et al., for example, antifuse 14 intervenes between single-crystal p-region 12 and polycrystalline n-region 16. The only exception Appellants can identify is described in column 3, line 65-68, where the antifuse separates an n-doped semiconductor layer from a conductor, forming a Schottky diode on rupture

of the antifuse. In this example as well, however, no diode exists before antifuse rupture, and the diode is formed by antifuse rupture.

Appellants believe the cited passage must be read in this context; that either layer 12 or 16 may be polysilicon, single crystal silicon, or metal, *so long as* a diode is formed upon rupture of the antifuse 14, as is clearly and repeatedly described throughout the rest of the patent. In contrast, Appellants find no embodiment in Zhang '396 in which a diode is formed upon rupture of the antifuse layer. The only embodiment of Zhang '396 that Appellants can identify that includes both an antifuse and a diode is shown in Fig. 9b. In this case the antifuse 502ca is formed between top conductor 501 and the p-n diode 502cb defined by n-doped layer 502cba and p-doped layer 502cbb. Unlike in all the embodiments of Mohsen et al., the diode 502cb of Zhang '396 is complete *as formed*, with the antifuse 502ca adjacent to it. It does not separate diode components as in every embodiment of Mohsen et al.

This structural difference will cause the antifuse devices of Zhang '396 and Mohsen et al. to have different electrical environments and behaviors before antifuse rupture. Simply put, before antifuse rupture, the devices of Figs. 9a, 10a and 10 of Zhang '396 et al. include a diode, while the devices of Mohsen et al. do not.

Due to the structural and electrical dissimilarity of the devices of Zhang '396 and of Mohsen et al., Appellants respectfully suggest that one skilled in the art would had have no motivation to replace the antifuse of Zhang '396 with the silicon nitride antifuse of Mohsen et al.

VIII. Conclusion

For the reasons set forth above, Appellants respectfully submit that Claim 1 is patentable over the proposed combination of Zhang '396 and Zhang '302, and that Claims 1 and 2 are patentable over the proposed combination of Zhang '396 and Mohsen et al. Accordingly, Appellants respectfully request removal of the 35 U.S.C. § 103(a) rejections of Claims 1 and 2.

Respectfully Submitted,

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Dated: April 7, 2008
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IX. Claims Appendix

The following claims are under appeal:

1. A three dimensional multi-level memory array disposed above a substrate, the array comprising:

   a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate;

   a second plurality of spaced-apart rail-stacks disposed above the first height and in a second direction different from the first direction; and

   a plurality of memory cells, each memory cell comprising a silicon nitride antifuse,

   wherein the antifuses are disposed at the intersections of the first rail-stacks and the second rail-stacks.

2. The array of claim 1, further comprising polysilicon p+n- diodes or polysilicon p-n+ diodes.

X. Evidence Appendix

None.

XI. Related Proceedings Appendix

None.